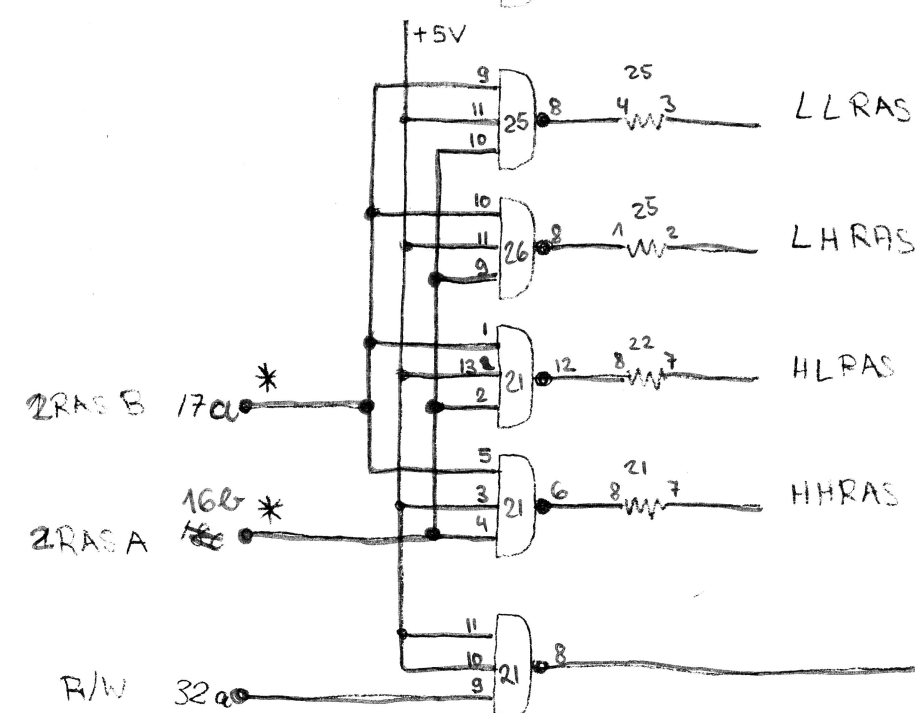


Hand-drawn schematic diagram of a 74F10 hex inverter. The chip is labeled '74F10' and 'U25'. It shows six inverters with inputs and outputs labeled. Inputs include 2C5B, 2C5A, 2C5L, 2C5H, 2C5C, and 2C5D. Outputs include 2C5B, 2C5A, 2C5L, 2C5H, 2C5C, and 2C5D. The diagram also shows power pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.




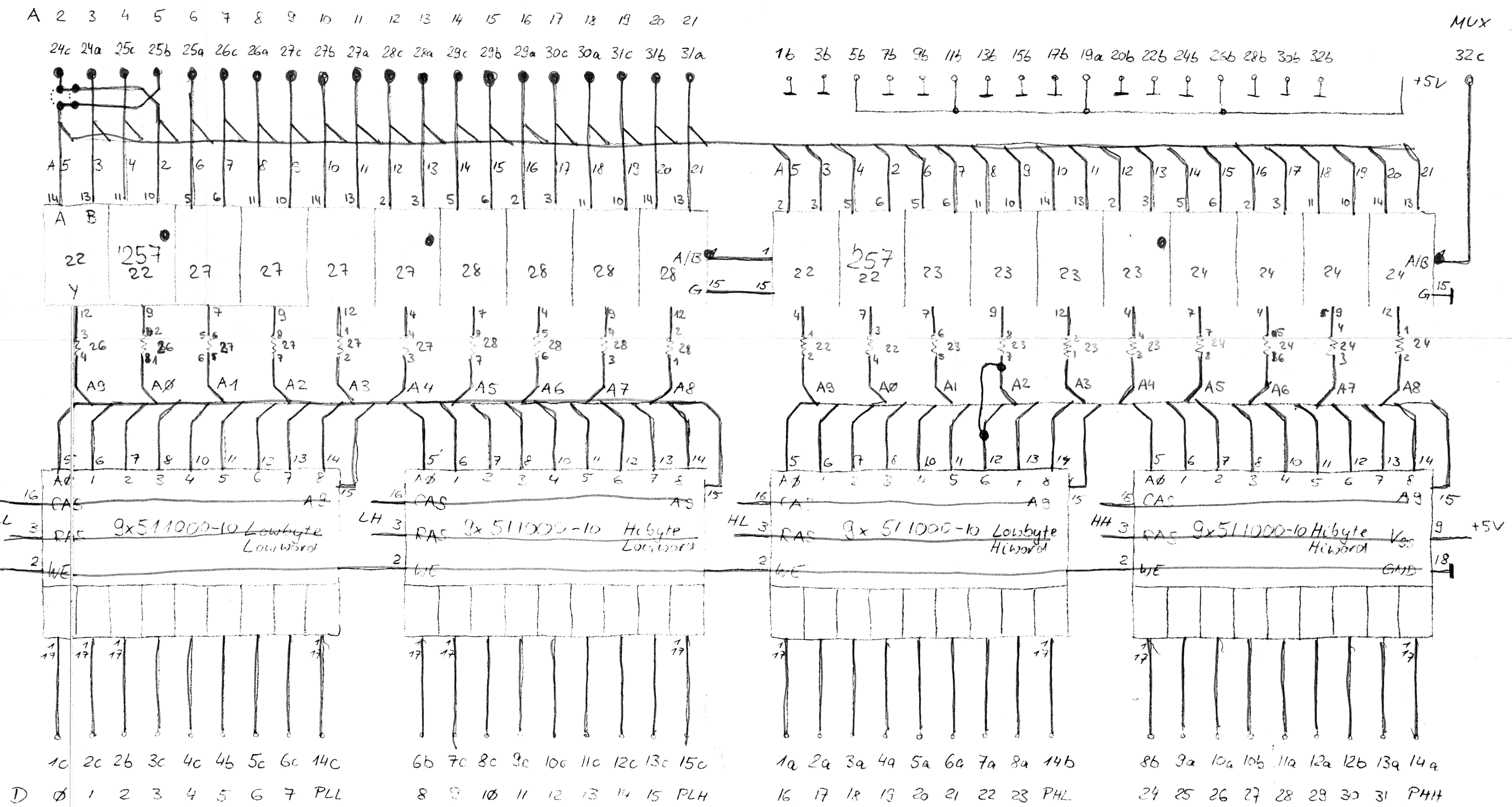
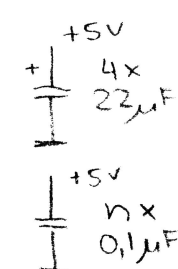
~~2CASS 19c \*~~  
~~2CASA 19b \*~~  
~~2RASS 19a \*~~  
~~2RASA 16b \*~~

2. 4 MB-Block

3. CASE 22a  $\frac{0}{*}$   
3. CASE 23b  $\frac{0}{*}$   
3. CASE 18a  $\frac{0}{*}$   
3. CASE 18b  $\frac{0}{*}$

~~ID 23a~~  JMP = 4MB

ID 23c  JMP = 12MB



Pin	A	B	C
1	D16	GND	D0
2	D17	D2	D1
3	D18	GND	D3
4	D13	E5	D4
5	D20	+5V	D6
6	D21	D8	D7
7	D22	GND	D5
8	D23	D4	D10
9	D25	GND	D11
10	D26	D27	D12
11	D28	+5V	D13
12	D29	D30	D14
13	D31	GND	D15
14	PHH	PHL	PLH
15	—	GND	PLH
16	—	2RASA	—
17	2RASE	GND	4RASE
18	3RASE	3RASA	4RAS A
19	+5V	2CASA	2CASE
20	CASHL	GND	CAS LL
21	CASHH	1CASA	CAS LH
22	3CASE	GND	1CASE
23	ID0	3CASA	ID1
24	A3	GND	A2
25	A6	A5	A4
26	A2	+5V	A7
27	A11	A10	A8
28	A12	GND	A12
29	A16	A15	A14
30	A18	GND	A17
31	A21	A20	A19
32	R/W	GND	MUX

[illegible]